

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yoshikazu KASUYA

Application No.: 10/690,023

Filed: October 22, 2003

Docket No.: 117576

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents

P.O. Box 1450

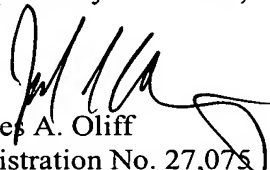
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. Relevance of reference No. 33 is discussed in the present specification.
- ☒ 3. The present application was filed or entered the U.S. National Stage of the PCT after June 30, 2003. In accordance with the June 11, 2003, Notice waiving the requirements of 37 C.F.R. §1.98(a)(2)(i), copies of any U.S. patents and patent application publications are not attached.
- ☒ 4. English-language Abstracts of the non-English language references Nos. 30-32 are attached hereto.
- ☒ 5. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office ([<http://www.jpo.go.jp>]), and is attached, but has not been reviewed for accuracy. See References 30-32.

Respectfully submitted,

  
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Date: March 22, 2004

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Form PTO-1449  
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US Dept. of Commerce  
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ATTY DOCKET NO.  
117576

APPLICATION NO.  
10/690,025

## INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

APPLICANT  
Yoshikazu KASUYA

FILING DATE  
October 22, 2003

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1	6,255,166 B1	07/03/2001	Ogura et al.		
	2	5,408,115	04/18/1995	Chang		
	3	5,969,383	10/19/1999	Chang et al.		
	4	5,422,504	06/06/1995	Chang et al.		
	5	5,494,838	02/27/1996	Chang et al.		
	6	6,177,318 B1	01/23/2001	Ogura et al.		
	7	6,248,633 B1	06/19/2001	Ogura et al.		
	8	US 2002-0100929	08/01/2002	Ebina et al.		
	9	US 2002-0127805	09/12/2002	Ebina et al.		
	10	6,413,821	07/02/2002	Ebina et al.		
	11	6,518,124	02/11/2003	Ebina et al.		
	12	US 2003-0054610	05/20/2003	Ebina et al.		
	13	US 2003-0057505	03/27/2003	Ebina et al.		
	14	US 2003-0058705	03/27/2003	Ebina et al.		
	15	US 2003-0060011	03/27/2003	Ebina et al.		
	16	US 2003-0190805	10/09/2003	Inoue		
	17	US 2003-0186505	10/02/2003	Shibata		
	18	US 2003-0166321	09/04/2003	Kasuya		
	19	US 2003-0157767	08/21/2003	Kasuya		
	20	US 2003-0166322	09/04/2003	Kasuya		
	21	US 2003-0166320	09/04/2003	Kasuya		
	22	US 2003-0211691	11/13/2003	Ueda		
	23	10/636,562	08/08/2003	Inoue		
	24	10/636,581	08/08/2003	Yamamukai		
	25	10/636,582	08/08/2003	Inoue		
	26	10/614,985	08/08/2003	Inoue		
	27	10/689,993	10/22/2003	Kasuya		
	28	10/689,987	10/22/2003	Kasuya		

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	29	10/689,990	10/22/2003	Kasuya		
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	30	JP A 2001-156188 (with abstract and translation)	06/08/2001	Japan		
	31	JP A 7-161851 (with abstract and translation)	06/23/1995	Japan		
	32	JP B1 2978477 (with translation)	09/10/1999	Japan		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)						
	33	Hayashi et al. "Twin MONOS Cell with Dual Control Gates", 2000 Symposium on VLSI Technology Digest of Technical Papers				
	34	Chang et al. "A New SONOS Memory Using Source-Side Injection for Programming", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, pp 253-255				
	35	Chen et al. "A Novel Flash Memory Device with S Plit Gate Source Side Injection and ONO Charge Storage Stack (SPIN), 1997 Symposium on VLSI Technology Digest of Technical Papers, pp 63-64				
EXAMINER				DATE CONSIDERED		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						

Date: March 22, 2004